

REMARKS

Claims 1-16 are pending. Claims 6-11 have been withdrawn from consideration. Reconsideration and allowance based on the comments below are respectfully requested.

Specification

The Office Action objects to claims 6-9 because the status was incorrectly identified. Applicants have noted that claims 6-9 have the status of “withdrawn” and will accordingly identify them as such in future Responses if necessary. Accordingly, withdrawal of the objection is respectfully requested.

The Office Action also objects to the Response filed January 23, 2006 under 35 U.S.C. §132(a) alleging it adds new matter. Specifically, the Office Action asserts that the term “ohmic contact” in claims 1, 12 and 13 is not supported by the disclosure. Applicants respectfully disagree.

The present invention is directed to passive matrix memories. Passive matrix memories have no switching elements (active regions). The word and bit lines form a continuous matrix where each crossing point creates a memory cell and can be individually accessed electrically which entails providing a voltage across the memory cell. Therefore each memory cell is in ohmic contact with a word and bit line in which a voltage differentially is applied at each memory cell. This is a fundamental understanding of passive matrix memories. A definition of ohmic contact is provided for the Examiner’s benefit. The definition was taken from McGraw-Hill Dictionary of Scientific and Technical Terms, Fifth Edition, page 1383. The definition states “a region where two materials are in contact, which has the property that the current flowing through it is proportional to the potential difference across it.” Thus, ohmic contact refers to materials being in contact and a voltage potential across the materials. In passive matrix memories, this is accomplished at all times as the crossing points of word lines and bit lines. This understanding of passive matrix memories is explained at least at page 2, lines 2-9 of applicant’s disclosure. Nonetheless, the understanding is inherent to passive matrix memories.

Accordingly, applicants respectfully submit that no new matter is added. Accordingly, withdrawal of the objection is respectfully requested.

§112, First Paragraph

The Office Action rejects claims 1, 2 and 13 under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement. Specifically, the Office Action asserts that the term “ohmic contact” is not described in the specification for one of ordinary skill to detect applicant’s had possession of the claimed invention. This rejection is respectfully traversed.

As noted above, the term “ohmic contact” although not stated in the specification is inherently implied and discussed in relation to passive matrixes. The fundamental design of the passive matrixes as compared with active matrixes is that passive matrixes require no active element and thus ohmic contact at all times on the word and bit lines forming the memory cells must be performed. The specification discusses this at least at page 2, lines 2-9 and throughout the specification in relation to the voltages applied at each memory cell. Therefore, one of ordinary skill would understand this feature of passive matrix memories as a fundamental feature and therefore recognize applicant’s have possession of this feature at the time of the invention. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

Prior Art Rejection

The Office rejects claims 1, 13, 14 and 16 under 35 U.S.C. §103(a) as being unpatentable over Kuroda (US 5,487,029) in view of Clemons, (US 4,599,709); claims 2-5 under 35 U.S.C. §103(a) as being unpatentable over Clemons, Kuroda and Dierke; and claims 12 and 15 under 35 U.S.C. §103(a) as being unpatentable over Kuroda, Clemons and Seyyedy (US 5,969,380). These rejections are respectfully traversed.

The applicant's claims recite a "passive matrix memory" and in previous response applicant's have argued against teachings applied by active matrix memories in Kuroda and Clemons. There is a fundamental difference between passive and active matrix memories. To further clarify the claims as being directed to passive matrix memories, applicant's amended the claims in the last Response filed on January 23, 2006, to recite that "each memory cell is at all times in ohmic contact with a word line and a bit line." Is a basic feature of passive matrix memories that cannot be taught by active or quasi active matrix memories.

Applicants respectfully submit that each of references Clemons and Kuroda teach an active matrix memory. Applicants respectfully submit that the references do not teach a passive matrix addressable memory with segmented word lines. Applicants note that in a passive matrix there are no switching elements, for example, switching transistors. This is to say that all memory cells are permanently in ohmic contact with the electrodes, i.e. the word lines and bit lines of the memory, such that when a single memory cell is selected for addressing, the operation can rise to sneak currents, voltage disturbs and stray capacitances. This is a problem pronounced in passive matrix addressable memories which is not as large of a problem in active memories. Thus, applicants embodiments are directed to addressing this problem by segmenting word lines addressing operations based on the segmentation.

In an ordinary active matrix addressable memory each ferroelectric capacitor has a single switching element corresponding thereto. Usually the switching element is a field effect transistor capable of connecting the word line with an electrode of the ferroelectric capacitor. When randomly addressing a memory cell in an active matrix addressable ferroelectric memory, only the memory cells selected for addressing will be in ohmic contact with both electrodes and only during the addressing operation. Therefore, this addressing will not evoke voltage disturbs in the matrix array and the unselected cells remain unaffected. Of course this arrangement requires large number of transistors creating a larger memory cell array and higher power consumption.

A solution to this problem, as disclosed in Kuroda is to employ memory units of the kind where one switching transistor is able to select more than one ferroelectric capacitor simultaneous. This of course means that one memory cell in the unit effected by the switching transistor is selected for an addressing operation and that the addressing operation can effect the other memory cells in the unit due to stray capacitances and voltage disturbs. For example, in Kuroda, a ferroelectric memory unit is comprised of eight memory cells in which one of the memory units is selected from the eight using the same switching transistor. In Kuroda, the memory is divided into separate memory blocks and as shown in Fig. 1, 16 memory blocks 00; 7, 7 thus forming a memory with 128 memory cells. The blocks are arranged to form columns of two blocks side by side and there is one sensing and writing means provided for each block in the module termed (WRCO) in Fig. 1. Each block contains 864 memory cells arranged in units of 8 sharing a common bit line and connectable via the switching transistor Q1 to a data line extending through and being common to both blocks in a column, i.e. Fig. 1, blocking 0, 0 and block 1, 0. Upon reading and writing a memory unit of each cell is selected via the selector to word line W1 and for a memory cell in the unit associated with the switching means Q1 can be addressed. The selection connects the bit line via the transistor Q1 with the data line D0 in this case one of the word lines W10....W17. A memory cell can be addressed for a read or write operation or either by the sensing means SA or write means WA, for which there is only provided one of each for each column of blocks.

Therefore, Kuroda is only able to address for read and write operations a single memory cell in a memory unit in one block at a time. However, in the case of having a memory with eight columns or blocks and one sense amplifier for each of the columns, the system can read in parallel eight memory cells, one from each block in a row. This, however, does not correspond to the word line segmentation of the present application.

Thus, Kuroda teaches a somewhat quasi active matrix in which the memory cells are separated into groups or units and a single switching transistor is activated for that particular group or unit. Thus, only that group or unit is in ohmic contact during the addressing of that particular memory unit in that group or unit. In contrast, in the passive matrix addressable memory of the present invention all memory cells can be affected not just those in a particular group or unit because all memory cells are in continuous ohmic contact. Further, the memory block arrangement is the not the same as the claimed word line segmentation in a passive matrix memory as claimed.

Further, Clemons fails to remedy Kuroda's deficiencies. Clemons is concerned with a static RAM memory. This is an active type of memory. In fact, Clemons specifically states at column 4, lines 13-17 that "typical static memory cells employ two cross coupled field effect transistors" and that "each cell typically includes two access transistors." The Examiner has stated that Clemons has been provided to teach particular sensing means which can be combined in a passive matrix memory. Applicants respectfully submit that Clemons does not teach separating word lines into segments as claimed by applicants. In applicant's invention, the word lines are segmented because of the unique nature posed by the passive matrix memories as discussed above. By segmenting the word lines which allows for selection of all bit lines associated with those word lines is that each bit line is then associated with a specific sensing amplifier and read out. In Clemons, each bite block is separated based on the bit lines. Each bit line is accessed using one of transistors T200 through T203 as illustrated for bite block one. The addressing of the voltage on the bit lines to specific sense amplifiers is not based on segmentation of the word lines. This is further noticed in Fig. 3 in which each segmented bit lines, referred to as bite block one through eight, is provided and connected to the IO switches. In segmenting based on the word lines, as in embodiments of the present invention, all bit lines across the entire array associated with those word line segmentations can be sent simultaneously at the associated sensing means. As illustrated in Fig. 3, only the specific bit lines associated with a particular bite block can simultaneously be sensed. This is accomplished for each bite block. Fig. 3 illustrates 4 bit lines and thus only four bit lines can be accessed at one time. In

contrast, if Clemons was segmented based on the word lines then all eight crossings of the bit lines with the word lines corresponding to bite blocks 1-8 would be simultaneously sensed for each word line in the word lines segmentation. This is not the case in Clemons as discussed above.

Thus, applicants respectfully submit that the problem remains of Kuroda and Clemons being associated with active passive matrixes in which continuous ohmic contact between the word lines and bit lines is not taught. Further, Clemons does not teach or suggest word line segmentation, let alone to be implemented in a passive matrix memory.

Therefore, the combination of Kuroda and Clemons fails to teach or suggest, *inter alia*, a passive matrix memory in which each memory cell is at all times a normal contact with a word line and a bit line and wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that the word line of the same position within each segment is sensed at the associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for a read out via the corresponding bit lines of the segment, as recited in claims 1 and 12.

Also, the combination of Kuroda and Clemons fails to teach or suggest, *inter alia*, a memory device having a first set of electrodes and a second set of electrodes with memory materials at all times in ohmic contact with the first and second set of electrodes and a number of sensing devices connected to each of the corresponding bit lines within each segment of word lines, where each word line in each segment is differentiated based on the position of the word line within the segment, each word line of each segment being adjoined to a separate bit line, such that the word line of the same position within each segment is sensed at an associated sensing device from the number of sensing devices, thus enabling simultaneous connection of all memory cells assigned to a segment, as recited in claim 13.

Further, Dierke and Seyyedy fail to remedy the deficiencies of Kuroda and Clemons. Accordingly, applicants respectfully submit that neither Kuroda, Clemons, Dierke or Seyyedy alone or in combination teach or suggest the above claimed limitations. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

Conclusion

For at least these reasons, it is respectfully submitted that claims 1-16 are distinguishable over the cited art. Further consideration and prompt allowance are earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. Billings (Reg. No. 48,917) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant respectfully petitions for a one (1) month extension of time for filing a reply in connection with the present application, and the required fee of \$60.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By 

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